



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Sayeed Ahmed et al.  
Application No. : 10/642,424  
Filed : August 14, 2003  
For : DUAL POWER MODULE POWER SYSTEM ARCHITECTURE

Art Unit : 2838  
Docket No. : 130209.507  
Date : January 12, 2004

Mail Stop Missing Parts  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents:

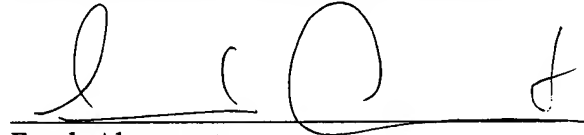
In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicants wish to make known to the U.S. Patent and Trademark Office the references set forth on the attached form PTO-1449. Applicants note that since the application filing date is after June 30, 2003, copies of the cited U.S. patents and published patent applications are not required and accordingly have not been provided. Copies of all other cited references are enclosed. As to any reference cited, applicants do not admit that it is "prior art" under 35 U.S.C. §§ 102 or 103, and specifically reserve the right to traverse or antedate any such reference, as by a showing under 37 C.F.R. § 1.131 or other method. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicants' duty to disclose all information they are aware of which is believed relevant to the examination of the above-identified application, applicants believe that their invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Applicants believe this Information Disclosure Statement has been timely filed, however, the Director is authorized to charge any fee due by way of this Information Disclosure Statement to our Deposit Account No. 19-1090.

Respectfully submitted,

Seed Intellectual Property Law Group PLLC

A handwritten signature in black ink, appearing to read 'Frank Abramonte', is written over a horizontal line.

Frank Abramonte  
Registration No. 38,066

Enclosures:

Form PTO-1449  
Cited References (16)

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EXPRESS MAIL NO. EV336613887US

Sheet 1 of 3

FORM PTO-144  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
130209.506APPLICATION NO.  
~~10/642,371~~ 10/642 424INFORMATION DISCLOSURE STATEMENT  
(Use several sheets if necessary)

APPLICANTS

Douglas K. Maly et al.

FILING DATE

August 14, 2003

GROUP ART UNIT

2838

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	4,142,231	02/27/79	Wilson et al.	363	141	
	AB	4,224,663	09/23/80	Maiese et al.	363	144	
	AC	4,458,305	07/03/84	Buckle et al.	363	141	
	AD	4,661,897	04/28/87	Pitel	363	17	
	AE	4,674,024	06/16/87	Paice et al.	363	71	
	AF	5,184,291	02/02/93	Crowe et al.	363	37	
	AG	5,172,310	12/15/92	Deam et al.	363	144	
	AH	5,230,632	07/27/93	Baumberger et al.	439	66	
	AI	5,243,757	09/14/93	Grabbe et al.	29	882	
	AJ	5,264,761	11/23/93	Johnson et al.	315	291	
	AK	5,395,252	03/07/95	White	439	66	

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
	AL	0 427 143 A2	05/15/91	DE (+ Abstract in English)		
	AM	0 578 108 A1	01/12/94	EP		
	AN	195 19 538 A1	11/28/96	DE (+ Abstract in English)		
	AO	9-117126	05/02/97	JP (+ Abstract in English)		
	AP					

## OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AQ	Kim, T-J, et al., "The Analysis of Conduction and Switching Losses in Multi-Level Inverter System," <i>IEEE</i> , pp. 1363-1368, 2001.
	AR	Mohan et al., <i>Power Electronics: Converters, Applications and Designs</i> , John Wiley & Sons Inc., USA, 1989, Chapter 26-8, "Circuit Layout," p. 654.

EXAMINER

DATE CONSIDERED

\* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).



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FORM PTO-144  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
130209.506

APPLICATION NO.

~~10/642,391~~ 10/642 427INFORMATION DISCLOSURE STATEMENT  
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2838

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	BA	5,422,440	06/06/95	Palma	174	133 B	
	BB	5,439,398	08/08/95	Testa et al.	439	801	
	BC	5,445,526	08/29/95	Hoshino et al.	439	69	
	BD	5,459,356	10/17/95	Schulze et al.	257	773	
	BE	5,508,560	04/16/96	Koehler et al.	257	730	
	BF	5,537,074	07/16/96	Iversen et al.	327	564	
	BG	5,559,374	09/24/96	Ohta et al.	257	723	
	BH	5,635,751	06/03/97	Ikeda et al.	257	584	
	BI	5,653,598	08/05/97	Grabbe	439	66	
	BJ	5,756,935	05/26/98	Balanovsky et al.	174	52.1	
	BK	5,847,951	12/08/98	Brown et al.	363	147	
	BL	5,938,451	08/17/99	Rathburn	439	66	
	BM	5,975,914	11/02/99	Uchida	439	66	
	BN	6,054,765	04/25/00	Eytcheson	257	724	
	BO	6,072,707	06/06/00	Hochgraf	363	71	
	BP	6,078,173	06/20/00	Kumar et al.	324	158.1	
	BQ	6,078,501	06/20/00	Catrambone et al.	361	704	

## OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

BS	Persson, E., "Power Electronic Design and Layout Techniques for Improved Performance and Reduced EMI," in <i>Proceedings of Power Electronics in Transportation, IEEE</i> , Dearborn, Michigan, October 20-21, 1994, pp. 79-82.
BT	Ratnayake, K. et al., "Novel Carrier PWM Scheme to Control Neutral Point Voltage Fluctuations in Three-Level Voltage Source Inverter," <i>IEEE Intl. Conf. on Power Electronics and Drive Systems</i> , PEDS '99, July 1999, Hong Kong, pp. 663-667.

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Sheet 3 of 3FORM PTO-1449  
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PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
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## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	CA	6,166,937	12/26/00	Yamamura et al.	363	141	
	CB	6,176,707	01/23/01	Neidich et al.	439	66	
	CC	6,212,087	04/03/01	Grant et al.	363	144	
	CD	6,292,371	09/18/01	Toner, Jr.	361	752	
	CE	6,434,008	08/13/02	Yamada et al.	361	728	
	CF	6,603,672	08/05/03	Deng et al.	363	37	
	CG	2002/0034088	03/21/02	Parkhill et al.	363	144	
	CH	2002/0126465	09/12/02	Maly et al.	361	818	
	CI	2002/0111050	08/15/02	Parkhill et al.	439	65	
	CJ	2002/0118560	08/29/02	Ahmed et al.	363	144	
	CK	2002/0167828	11/14/02	Parkhill et al.	363	144	
	CL	10/642,424		Ahmed et al.			08/14/03
	CM	60/233/992		Ahmed et al.			09/20/00
	CN	60/233,993		Ahmed et al.			09/20/00
	CO	60/233,994		Ahmed et al.			09/20/00
	CP	60/233,995		Ahmed et al.			09/20/00
	CQ	60/233,996		Ahmed et al.			09/20/00
	CR	60/471,387		Ahmed et al.			05/16/03

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
	CS					

## OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	CT	Seo, J. et al., "A New Simplified Space-Vector PWM Method for Three-Level Inverters," <i>IEEE Transactions on Power Electronics</i> 16(4):545-550, July 2001.
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